

→ Fig. 1b

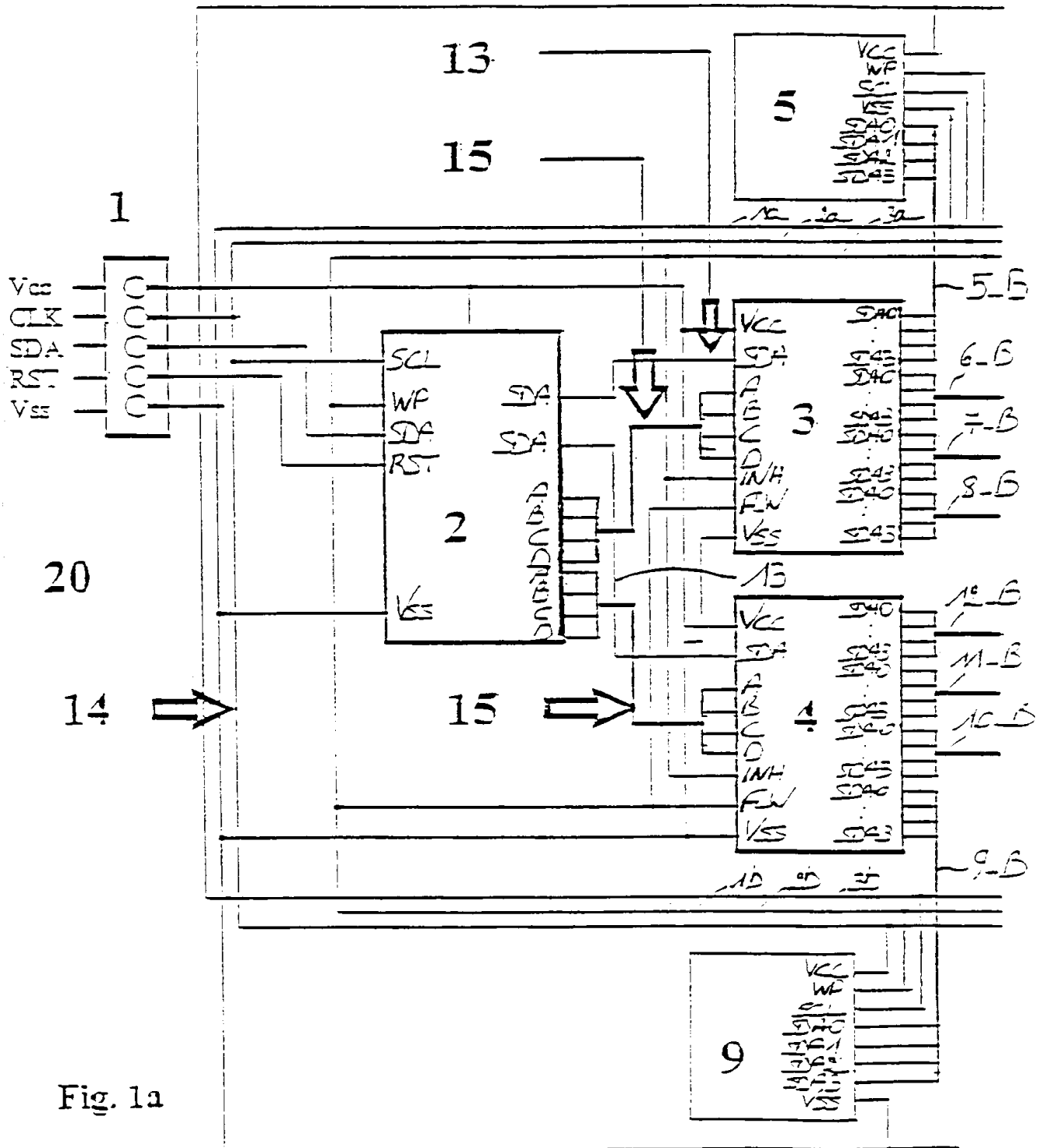


Fig. 1a

→ Fig. 1c

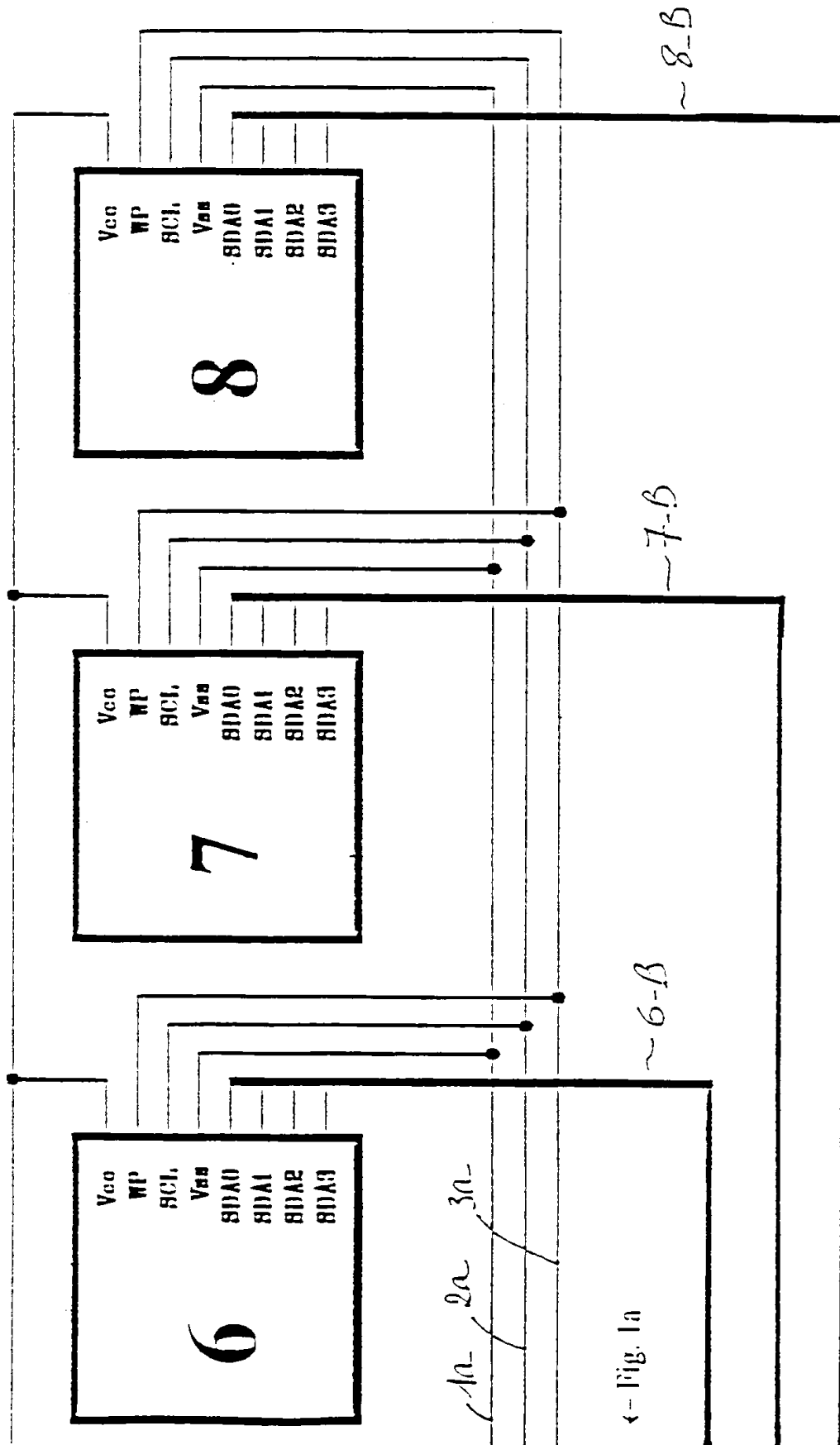


Fig. 1b

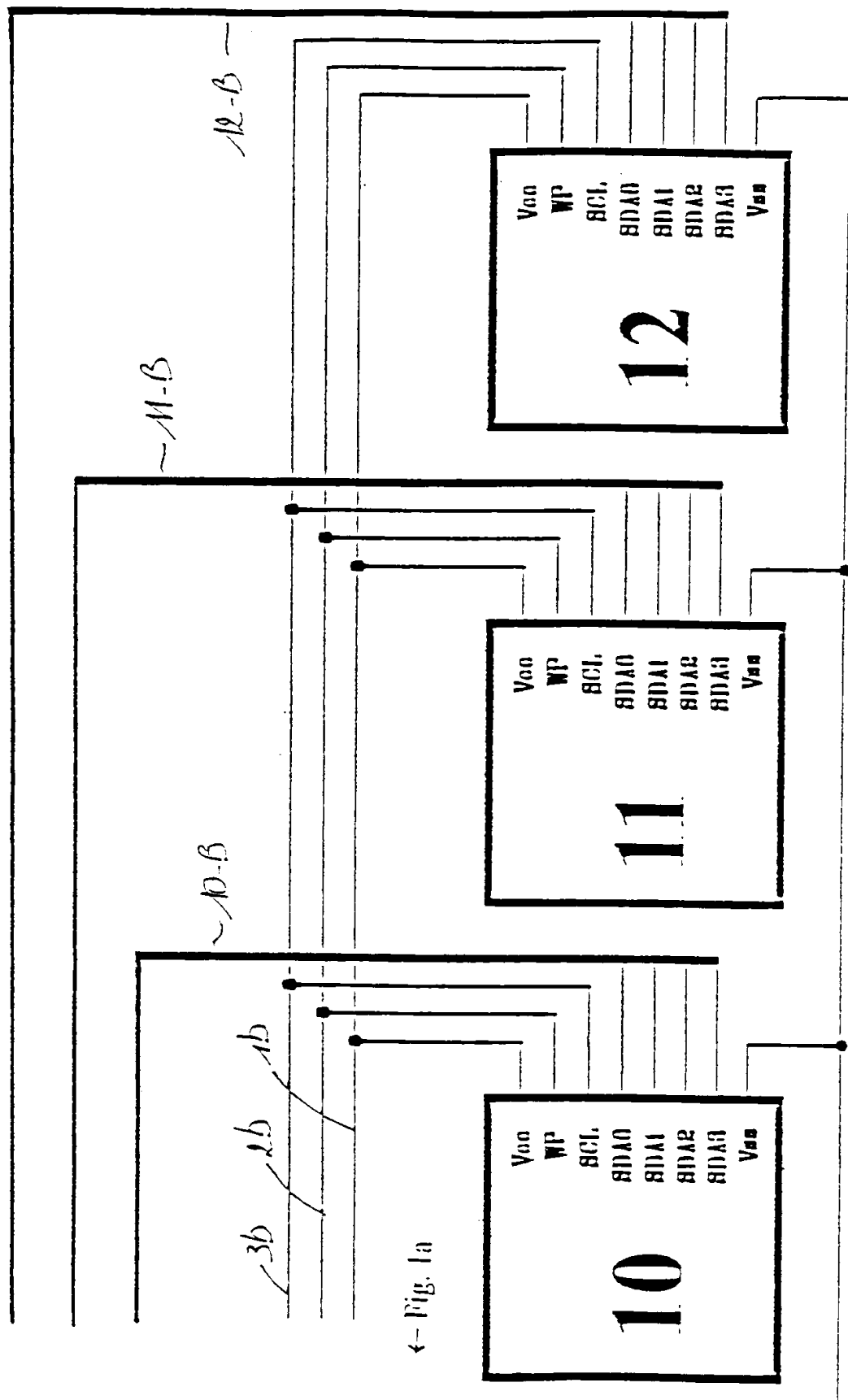


Fig. 1c

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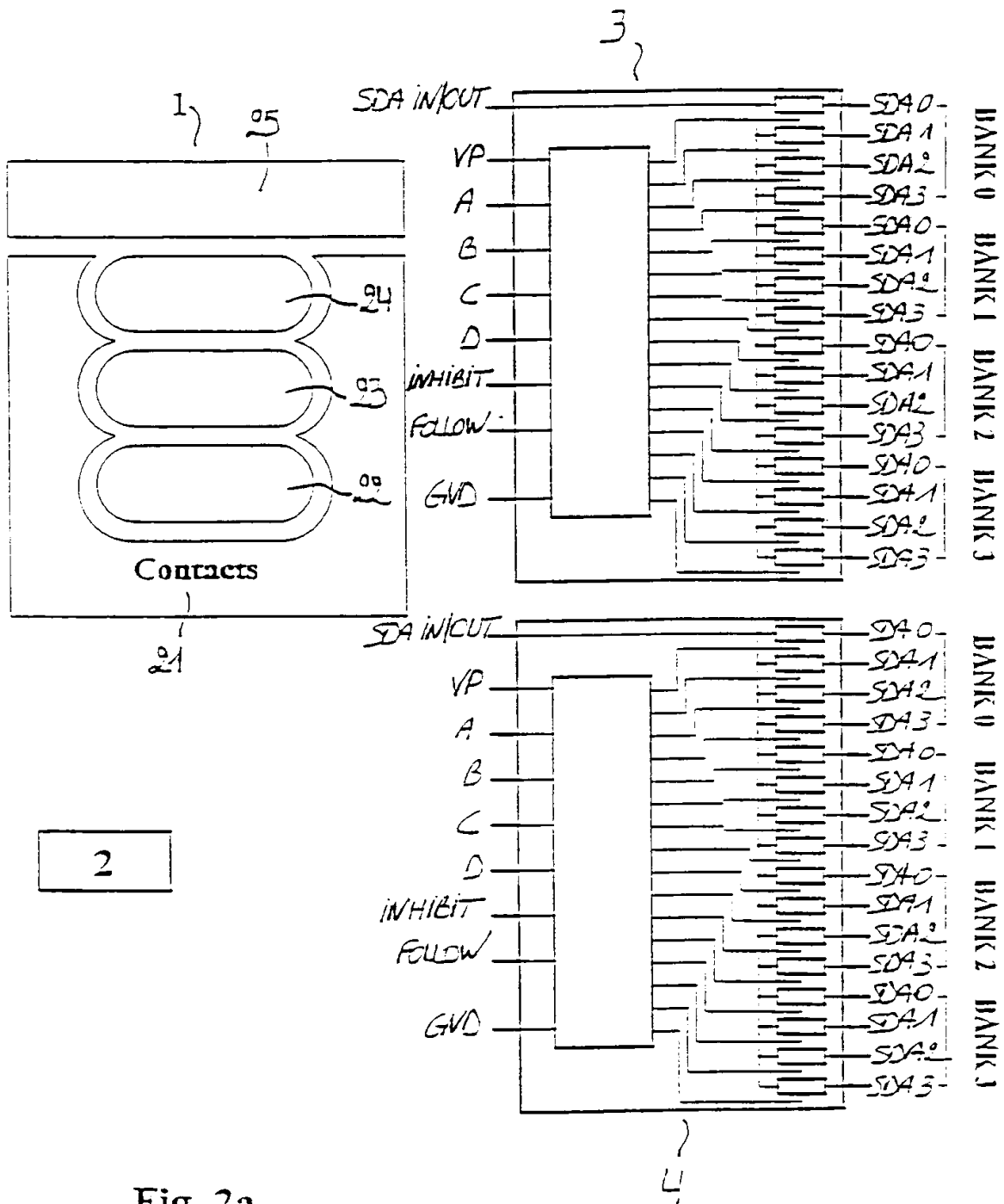


Fig. 2a

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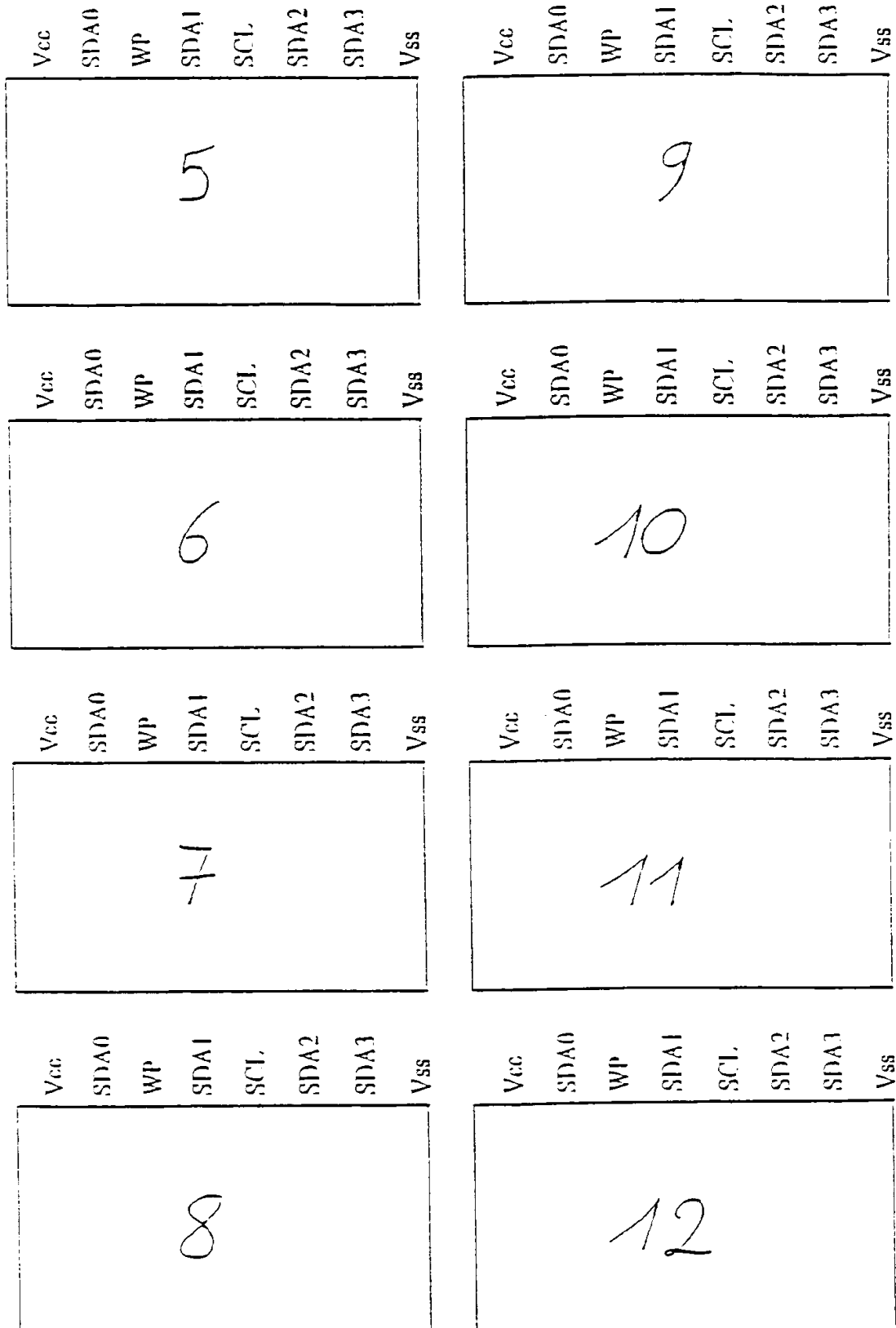
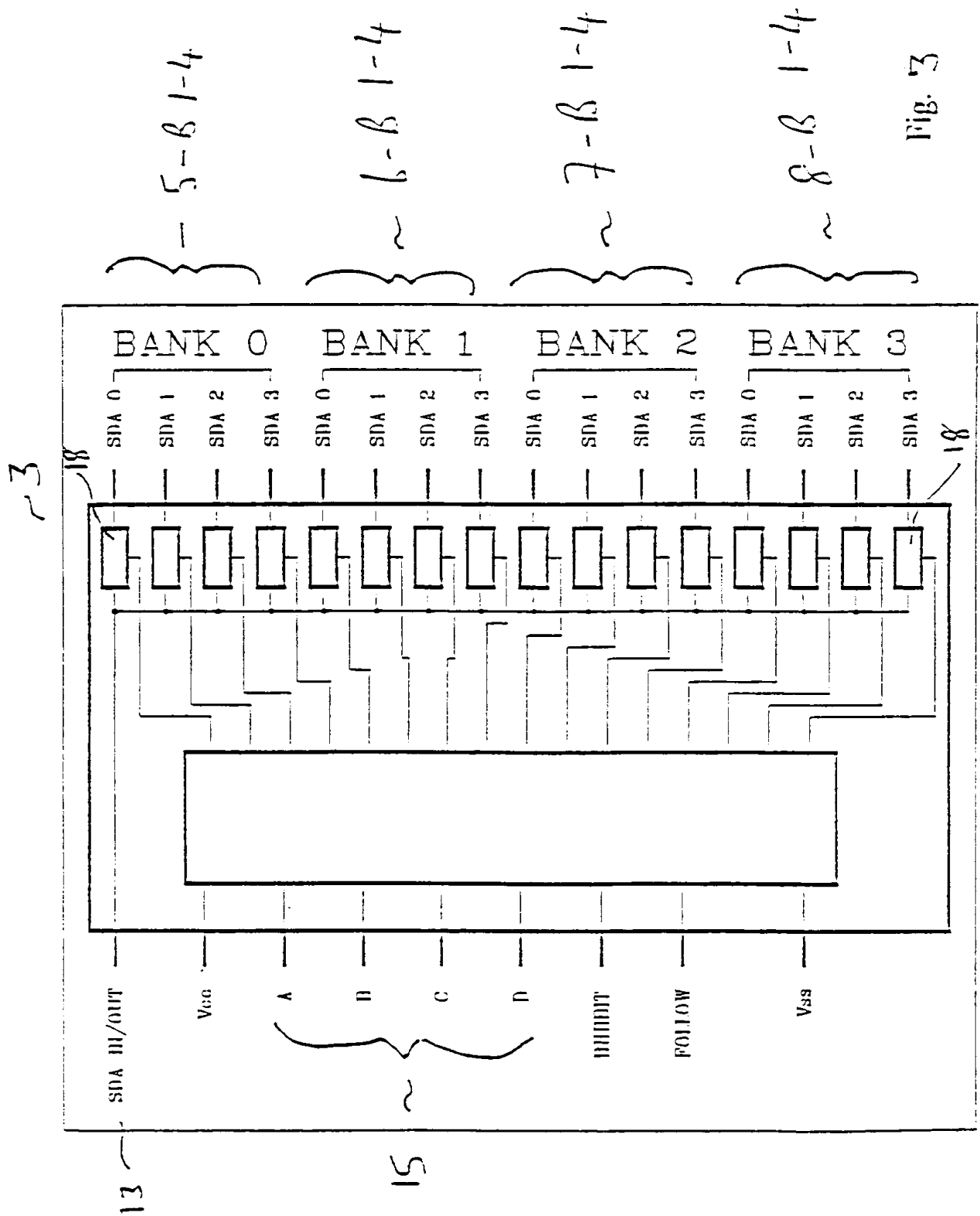
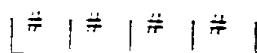


Fig. 2b

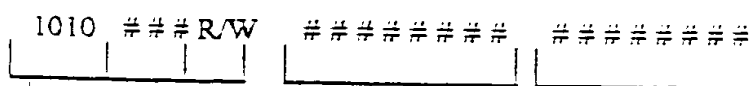


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4 bit parallel address portion defines one of the serial outputs of the dispatcher. Each serial output is connected to one memory unit

Fig. 4A



Three bit code to determine which of the eight 64 kbyte EEPROM memories is addressed

4 bit control nibble which determines any suitable parameter, e.g. a manufacturer's code

read/write control bit

Address high byte for specifying one byte of 64kbyte EEPROM

Address low byte for specifying one byte of 64 kbyte EEPROM

Fig. 4B

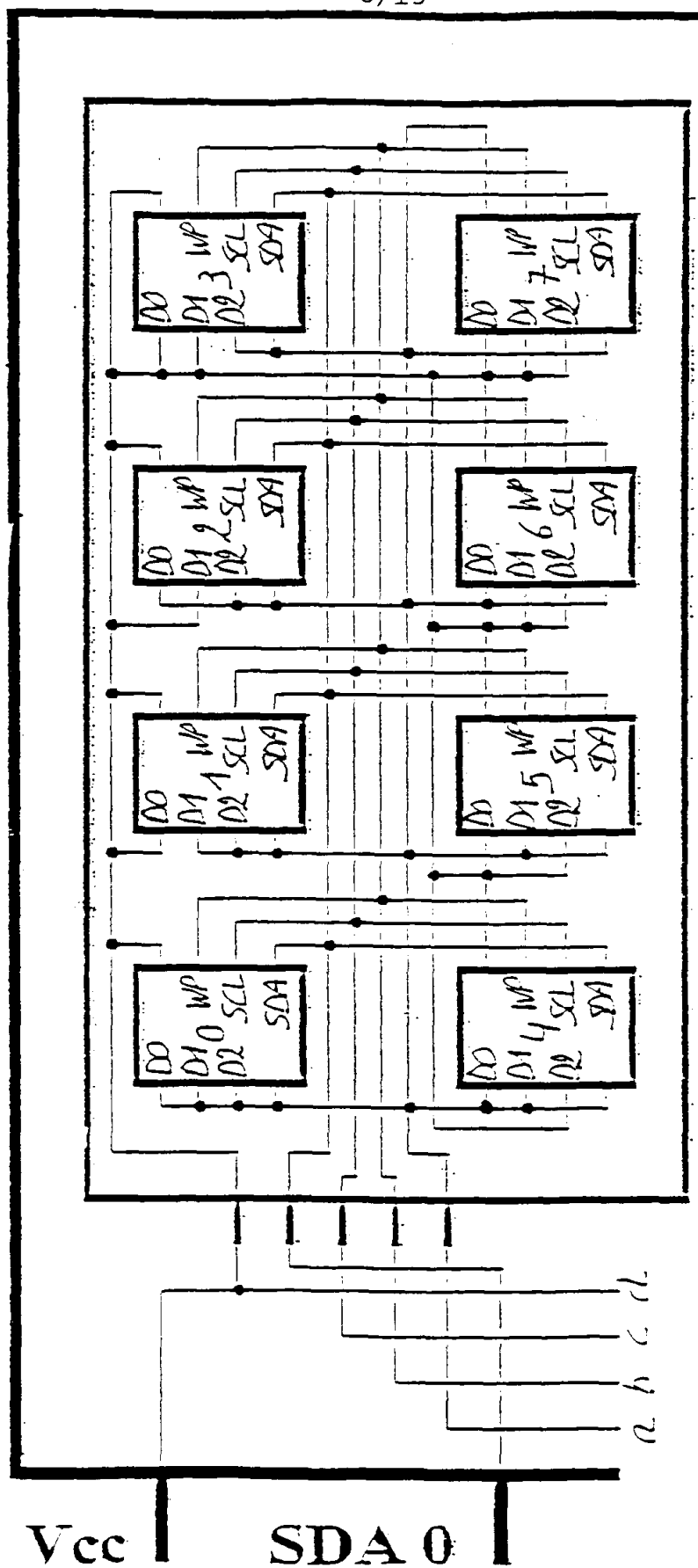
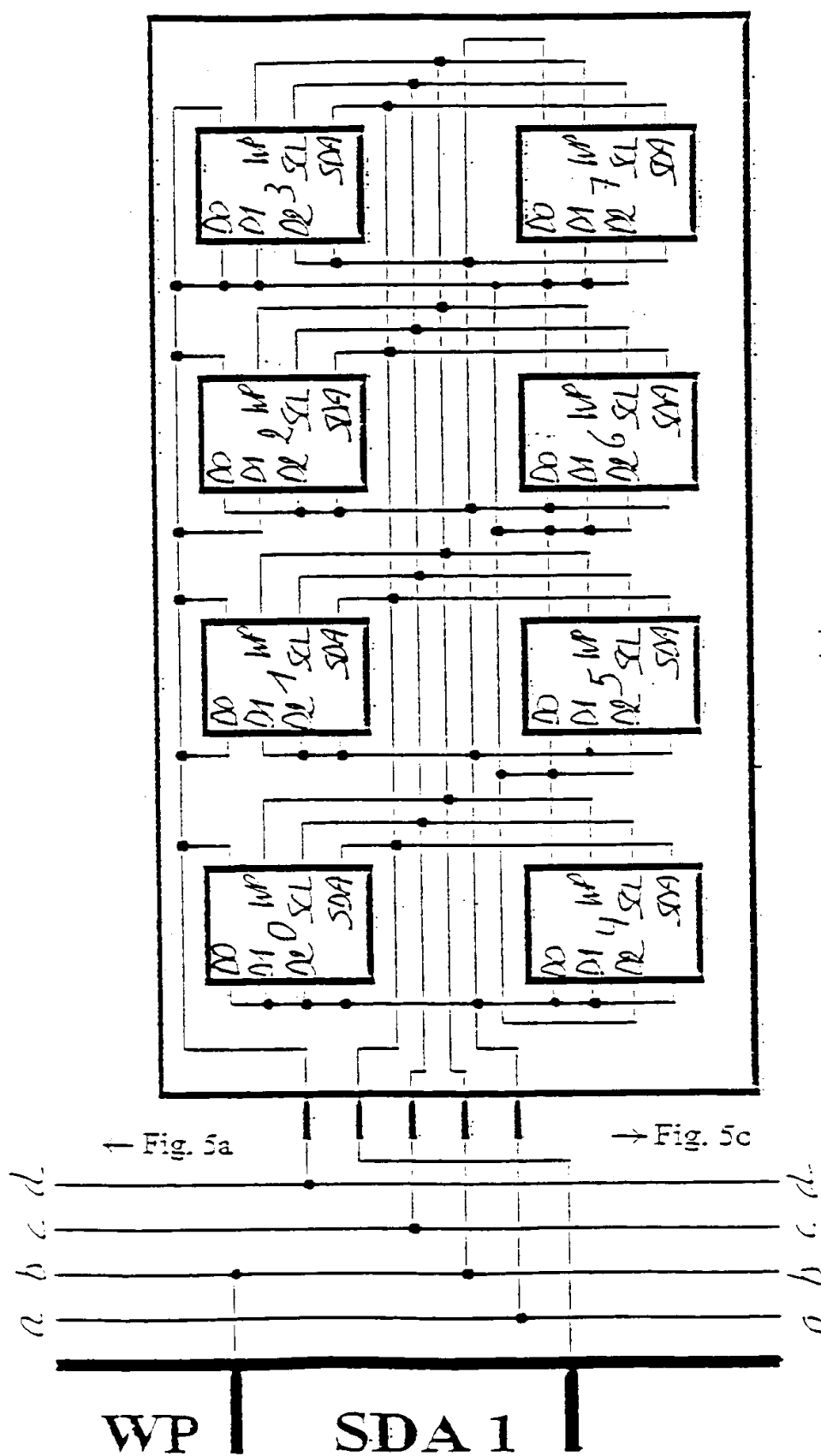


Fig. 5a

Fig. 5b





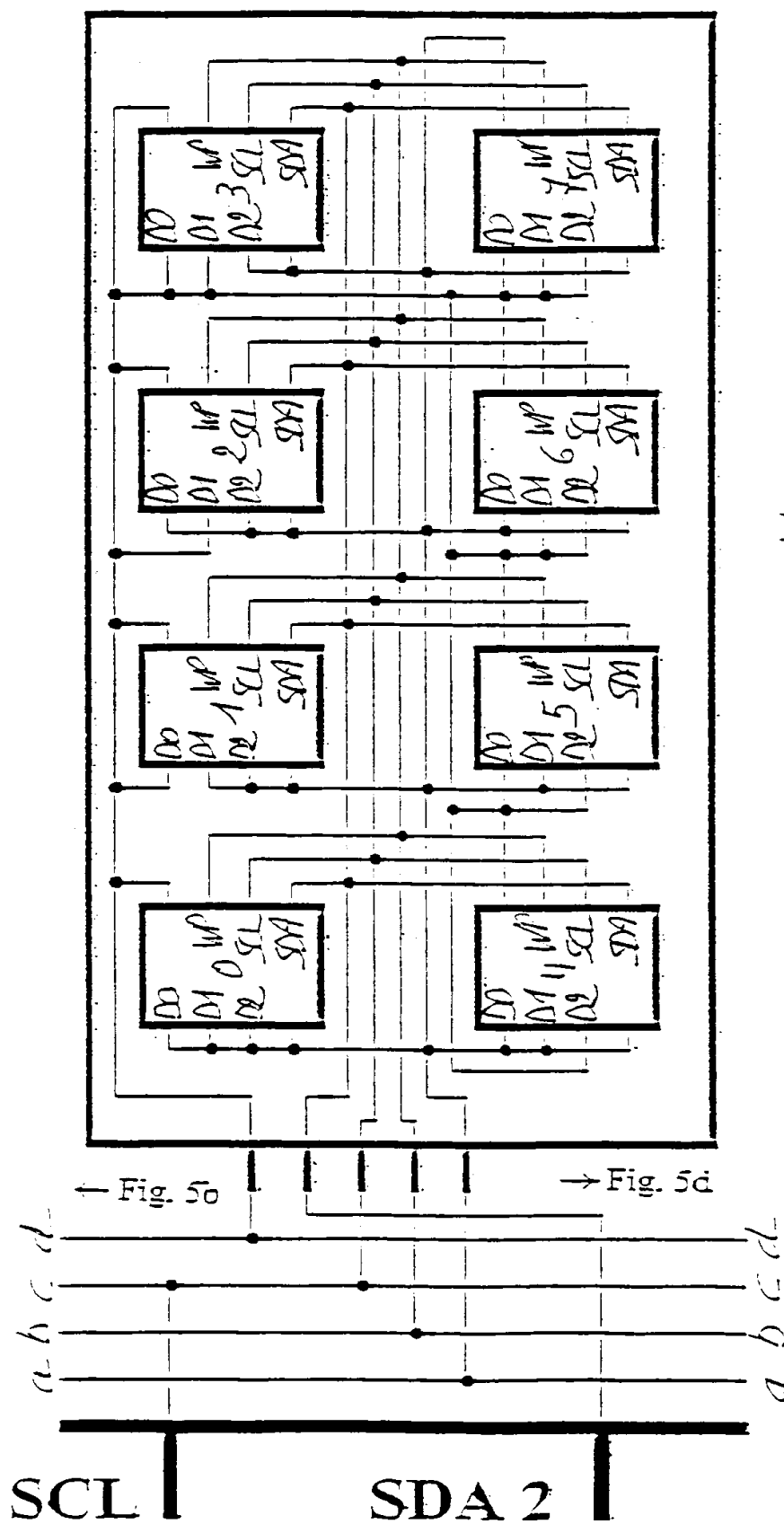
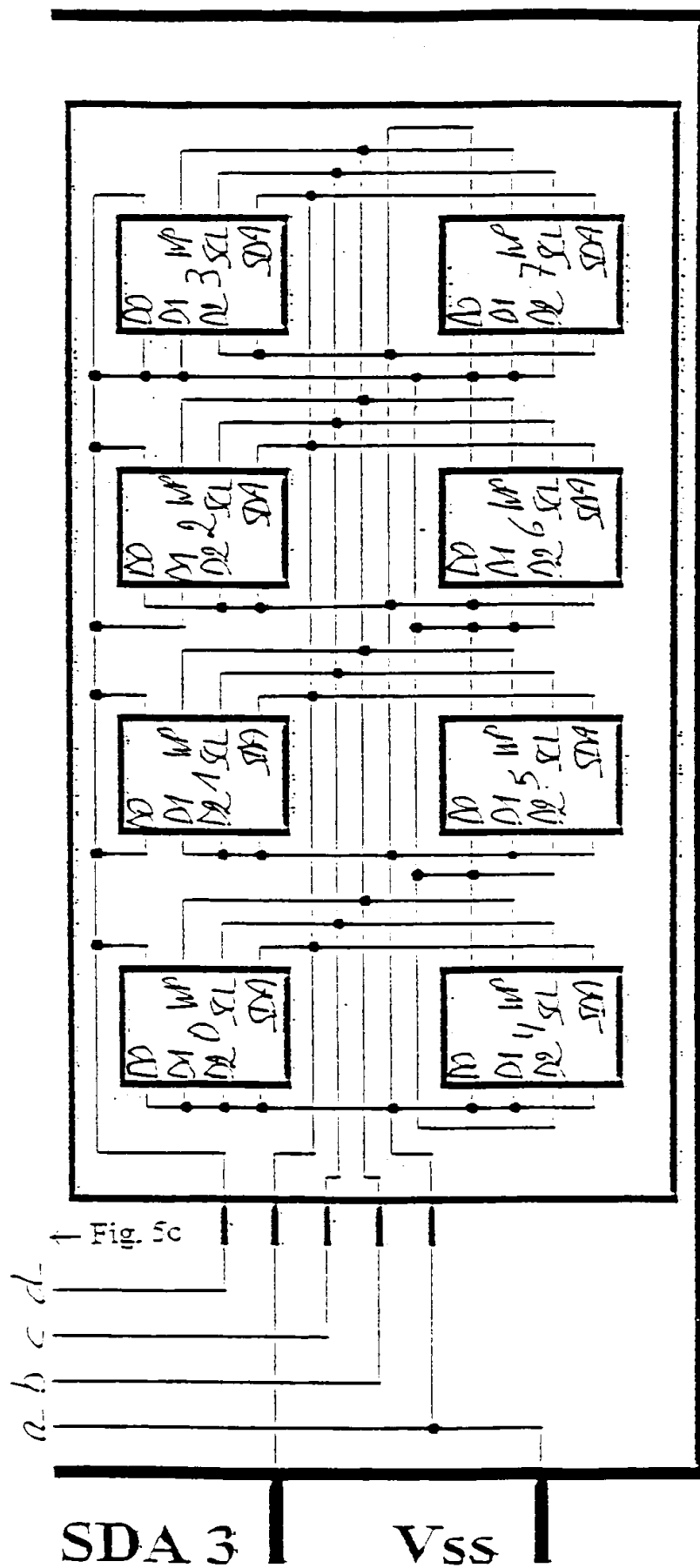


Fig. 5c



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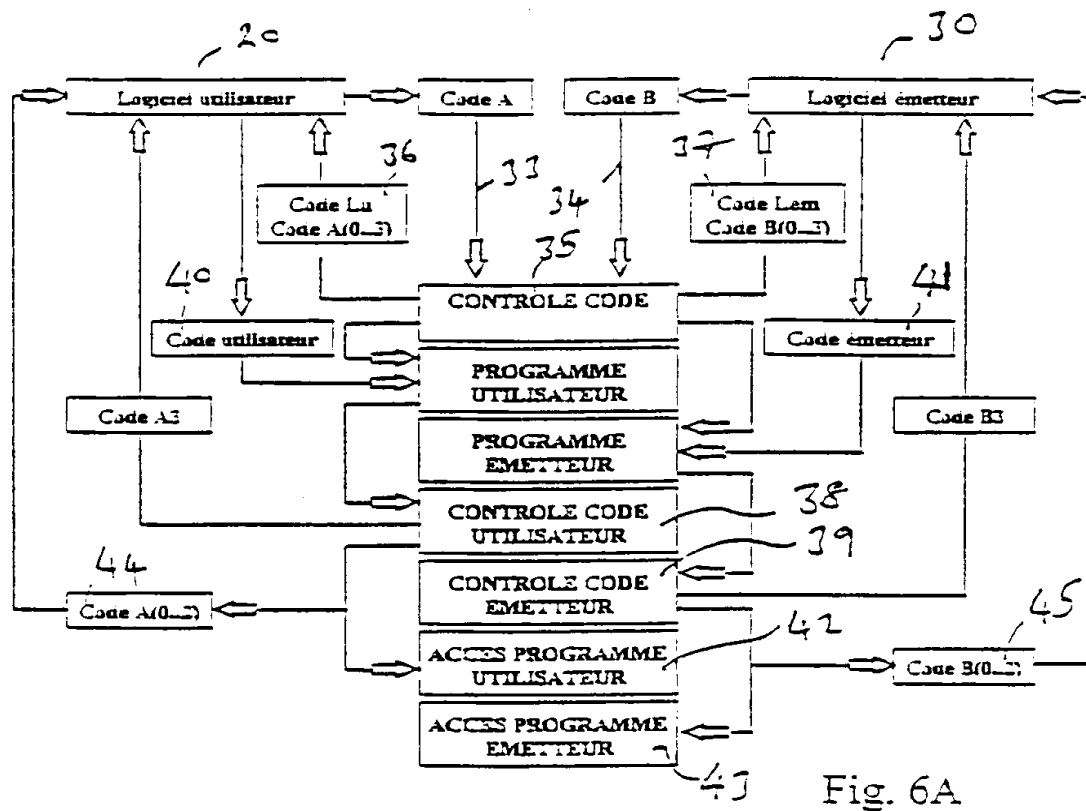


Fig. 6A

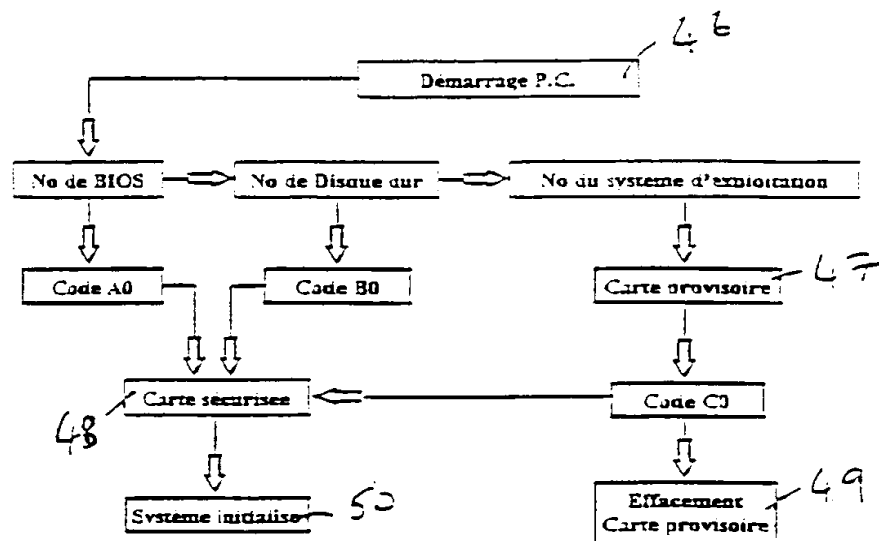


Fig. 6B

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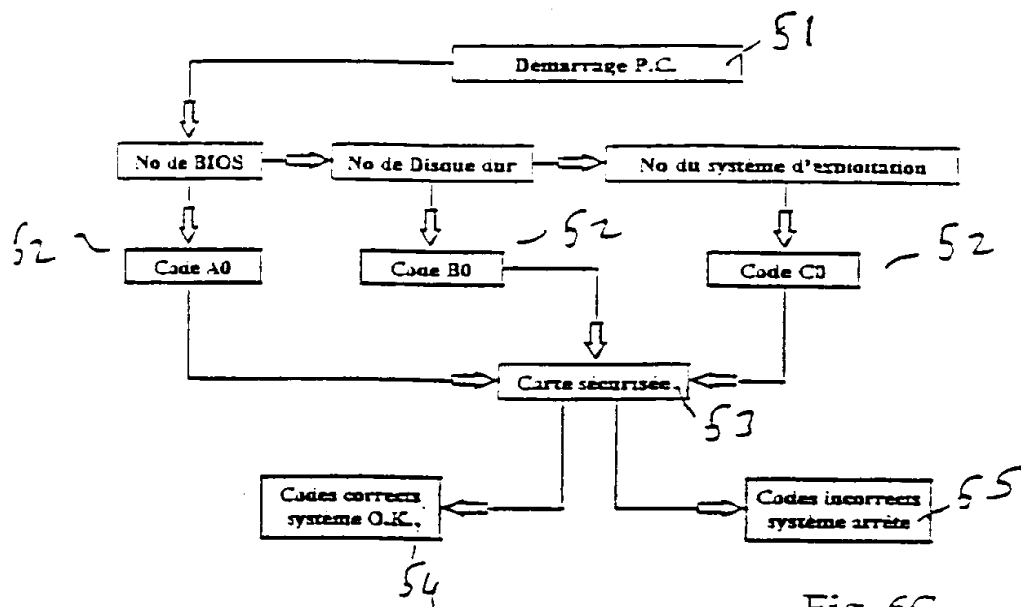


Fig. 6C

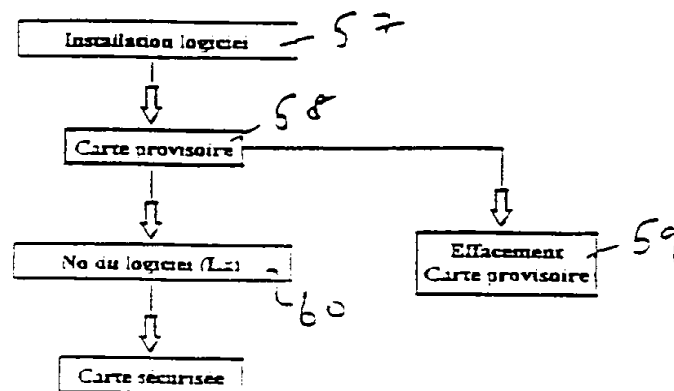


Fig. 6D

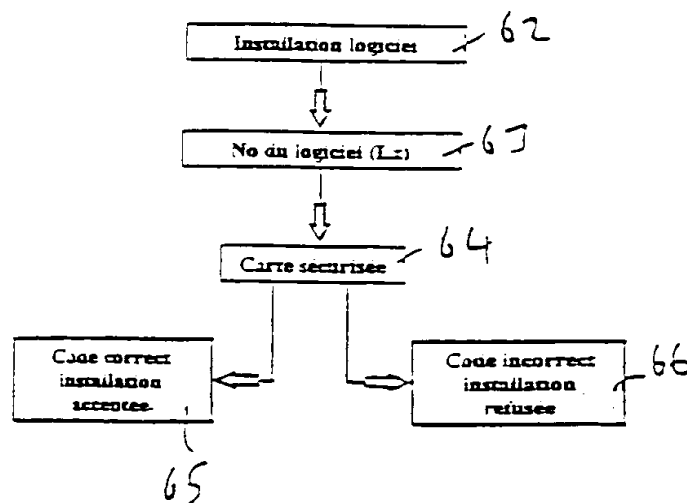


Fig. 6E

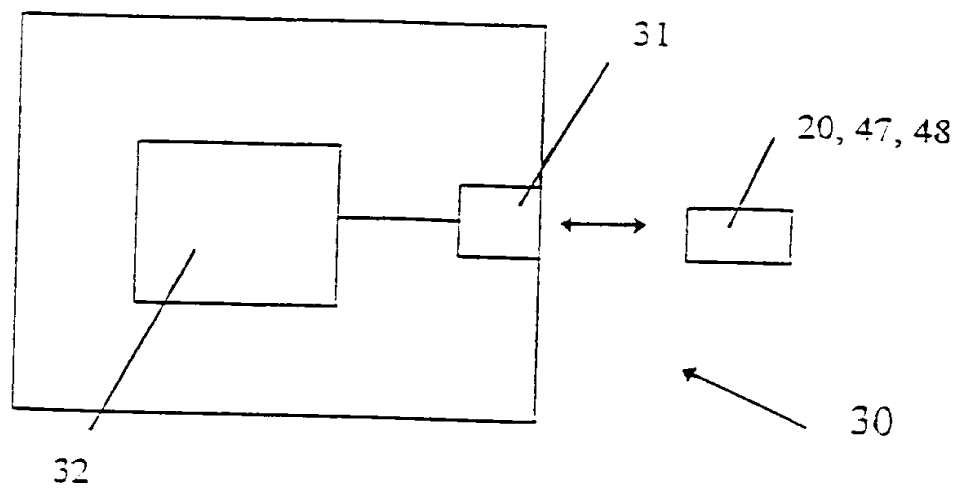


Fig. 7

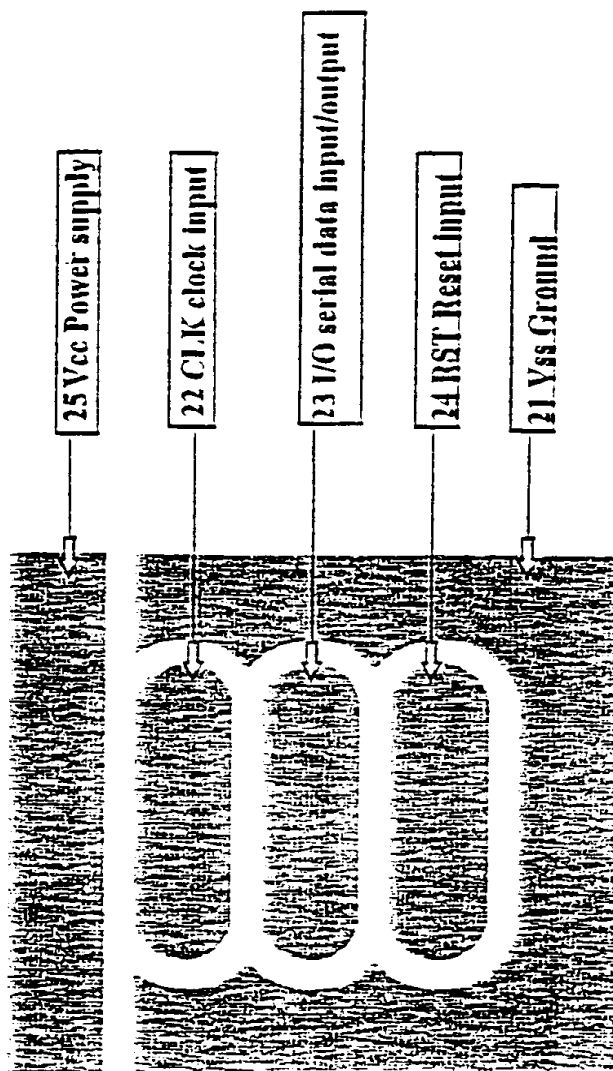


Fig. 8